B.E. / B.Tech. Computer Science & Engineering (Model Curriculum) Semester-III

SE104CS - Digital Electronics

P. Pages : 2 **GUG/S/25/13804N**

Time : Three Hours * 2 2 5 7 * Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Due credit will be given to neatness and adequate dimensions.
3. Assume suitable data wherever necessary.
4. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Prove NOR gate as universal gate. **4**

b) Convert the following- **6**

i) $(2637)10 = (?)9's$ complement

ii) (143)10 = (?) Excess-3

iii) $(111 \cdot 1010)2 = (?)10$

c) Define the following terms Fan out, Propagation delay and Noise margin. **6**

OR

2. a) Solve- **4**

i) $10111 \cdot 101 + 110111 \cdot 01 = ?$

ii) $1100 \cdot 10 - 111 \cdot 01 = ?$

b) Simplify $F(A,B,C) = AB + AB'C + AB'C'$ using Boolean algebra. **4**

c) A quad two-input AND gate has following parameters VOH(min.)=2.7V, VOL(max.)=0.4V, VIH (min.)=2V, VIL (max.)=0.8V, Vcc=5.0V, ICCH= 18mA, ICCL=32mA, tpLH=4.5 ns and tpHL=5.0 ns. Determine the Speed-Power product and Noise Margin. **8**

3. a) Minimize using $K - Map\ F = \Sigma m$ (0, 13, 14, 15) + d (1, 2, 3, 9, 10, 11). **6**

b) Realize 4-bit Carry Look Ahead Adder with look ahead carry generator. **10**

OR

4. a) Implement even parity generator and Checker for a 3-bit binary message. **8**

b) Design BCD to excess-3 code convertor. **8**

5.	a)	What is race around condition in JK Flip-Flop? How it can be avoided.	**4**
	b)	Convert SR flip flop to JK Flip Flop.	**6**
	c)	Elaborate 3-bit twisted ring counter with its waveform.	**6**

OR

6.	a)	Design a type T counter that goes through states 3, 4, 2, 1, 3, ----. Is the counter self starting.	**8**
	b)	Design a sequence generator that generates the sequence "100010011010111"	**8**
7.	a)	Explain the operation of Sample and hold circuit with diagram? Why Sample and hold circuit is used in ADC.	**8**
	b)	Define resolution of DAC. How will you improve it? Determine the resolution of 16 bit DAC in percentage.	**8**

OR

8.	a)	What are the disadvantage of binary weighted DAC.	**6**
	b)	Explain the Successive approximation ADC with suitable diagram. What is the resolution of 12 bit Successive approximation ADC?	**10**
9.	a)	Compare PAL and PLA.	**4**
	b)	Compare CPLD and FPGA.	**4**
	c)	Implement 4-bit Binary to grey code convertor using MOSFET ROM.	**8**

OR

10.	a)	Implement BCD to Excess-3 code convertor using bipolar transistor PROM.	**8**
	b)	Draw and explain the architecture of a FPGA? Explain with example how LUTs are configured to implement a design.	**8**

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